DSPChip: SoC for Audio Applications – Tapeout in Intel 16

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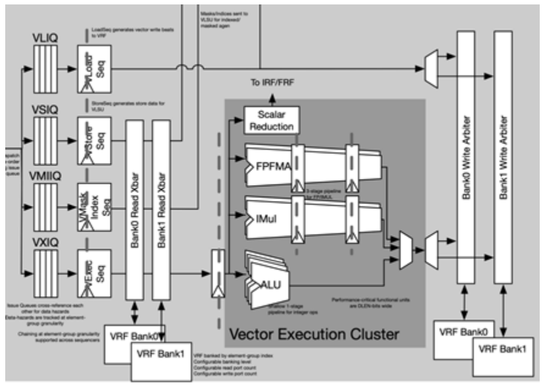
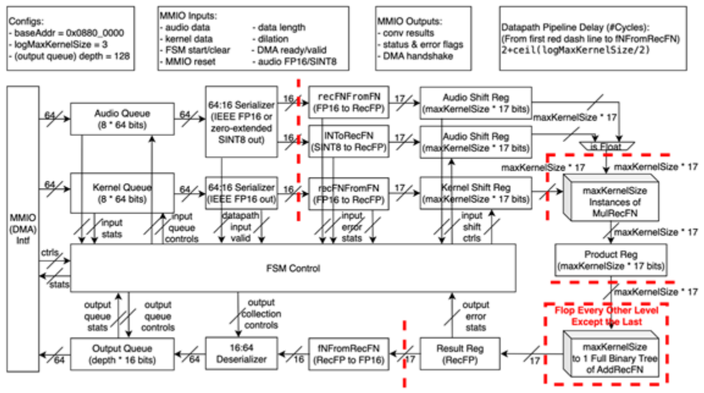
Saturn Vector Cores

- Rocket **in-order** cores with **256-bit Saturn Vector units**
- Direct-mapped 4 KiB ICache & 4 KiB DCache
- Minimal area configuration targeting integer operations
- RISC-V Vector Extension Version 1.0 compliant



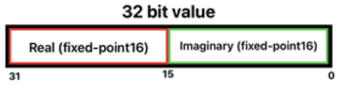
Convolution Accelerator

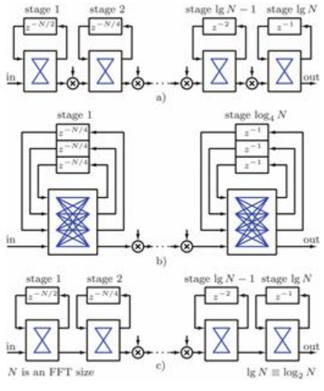
- **1D dilated conv. engine** to alter, classify, and detect audio
- Fully custom design that contains four pipeline stages, mixed width queues, audio input format toggle, and parameterized scalability
- 190x performance speedup over Rocket core



SDF-FFT Accelerator

- Chipyard integration of the 128-bit **SDF-FFT generator** by Vladimir Milovanović and Nikola Petrovic
- Drastically smaller than the chipyard FFT generator
- Custom TileLink Front-end with input and output buffers

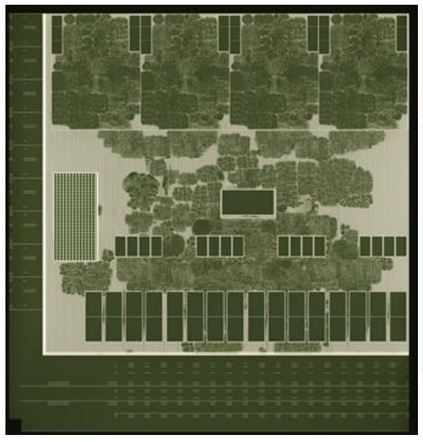


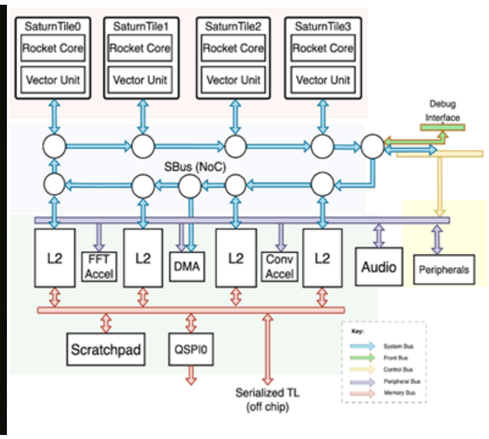


A Highly Parametrizable Chisel HCL Generator of Single-Path Delay Feedback FFT Processors

Overview

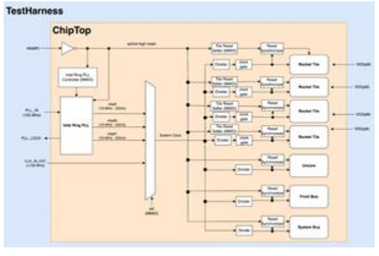
- Design and tapeout a **RISC-V SoC** suitable **for audio effects processing applications** in Intel 16
- Feature new custom designs of SDF-FFT, convolution accelerators, and general DMA engine targeting audio application performances
- Design and integrate a fully custom **8-channel audio subsystem**
  - Consist of I²S audio interface and Sigma-Delta DAC
- Improve compute performance by integrating Saturn vector units on four in-order rocket tiles that optimize VLEN=128, 256 instr.
- 32KB scratchpad, 256KB L2, and all four Saturn vector cores on a 128-bits Constellation 1D torus NoC
  - Upgrade from 64-bits in previous tapeout iterations
- 19x GPIO, 4x I²S, 2x ΔΣ DAC, 4x PWM, 3x UART, 2x QSPI, 1x SPI, 2x I²C, 1x 8-bit SerialTL, 1x 1-bit Peripheral SerialTL, 1x JTAG





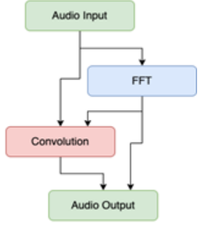
Clocking Spec

- DSP top level operates at 500MHz clock, generated by Intel Ring PLL
- The Internal ring oscillator provides clocks from 10MHz to 2GHz, tunable via custom MMIO interface
- Externally controlled clock muxes to support post-silicon debug



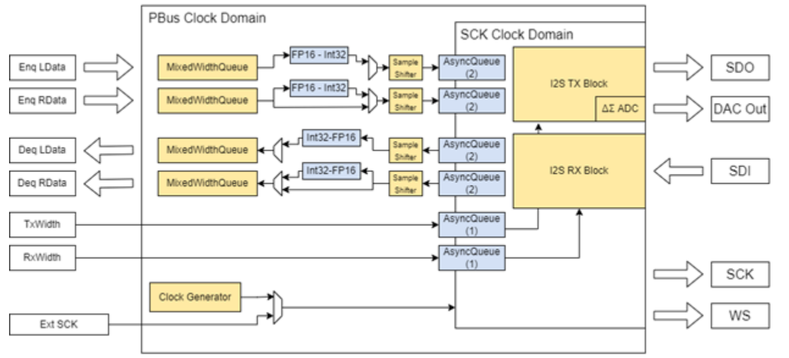
Next Steps

- **Bringup and validate taped out functionality**
- Investigate basic digital signs of life
- Validate digital accelerators and cores, new audio IO peripherals and non-core peripherals
- Verify clock and power subsystems
- Test QSPI and JTAG boot



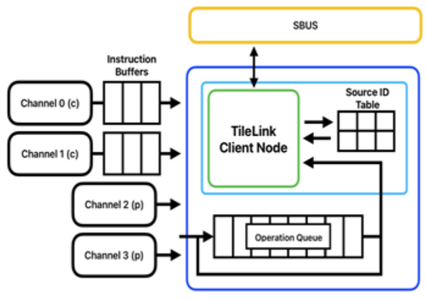
Audio Interface

- 8 Channel Full-Duplex Audio Interface
- Stereo Delta-Sigma DAC for audio output without external components
- 4 Independent Stereo I²S Channels for External CODECs
- 8,16,24,32 Bit Int or FP16 Samples supported for Tx + Rx
- 120Hz-4MHz Sample Rate w/ internal clock
- Supports I²S Peripheral mode w/ external clock source
- Programmable Watermark signal for DMA audio control



DMA Engine

- General DMA built for:
  - Memory → Memory
  - Peripheral → Memory
  - Memory → Peripheral
- Config contains:
  - 3 CPU Channels
  - 4 Peripheral Channels
  - 8 In-flight Instructions



- Supports:
  - Multiple channels with load balancing and Double-buffering
  - Peripheral polling
  - Variable transfer width/length
  - Variable stride on read and write
  - Multiple inflight operations

Acknowledgements

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